AMENDMENTS IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A straddled gate device formed on a semiconductor-on-insulator (SOI) substrate having active regions defined by isolation regions and an insulator layer, the device comprising:

a first gate defining a first channel region interposed between a source and a drain formed within the active region of the SOI substrate;

a second gate straddling the first gate defining second channel regions interposed between the first channel region and the source and the drain;

a contact connecting the first gate with the second gate;

a first dielectric layer separating the first gate from the SOI substrate, the first dielectric layer having a relative permittivity greater than SiO_2, and

a second dielectric layer separating the second gate from the SOI substrate, the second dielectric layer having a relative permittivity less than the first dielectric layer.

2. (Previously Presented) The straddled gate device according to claim 1, wherein the first gate defines a work function and the second gate defines a second work function, and

the second work function is less than the work function of the first gate.

3. (Original) The straddled gate device according to claim 2, wherein the second work function of the second gate is 0.3 – 0.5 eV less than the work function of the first gate.

4. (Original) The straddled gate device according to claim 1, wherein the source and the drain include main source and drain regions and source and drain extension regions.

5. (Previously Presented) The straddled gate device according to claim 1, includes a silicide layer formed on the source and the drain.

6. (Previously Presented) The straddled gate device according to claim 5, wherein the silicide layer which is formed on the source and the drain has a thickness in a range between 100 Å and 400 Å.

7. (Previously Presented) The straddled gate device according to claim 5, including a second silicide layer formed on electrodes of the second gate.

8. (Previously Presented) The straddled gate device according to claim 7, wherein the second silicide layer formed on the electrodes of the second gate has a thickness in a range between 100 Å and 400 Å.

9. (Previously Presented) The straddled gate device according to claim 7, wherein the silicide layer formed on the source and the drain and the second silicide layer formed on the electrodes of the second gate are of silicide of different species.

10. (Previously Presented) A straddled gate device formed on a semiconductor-on-insulator (SOI) substrate having active regions defined by isolation regions and an insulator layer, the device comprising:

a first gate defining a first channel region interposed between a source and a drain formed within the active region of the SOI substrate;

a second gate straddling the first gate defining second channel regions interposed between the first channel region and the source and the drain; and

a contact connecting the first gate with the second gate,

wherein the semiconductor-on-insulator substrate is a germanium-on-insulator (GOI) substrate.

11. (Previously Presented) The straddled gate device according to claim 10, further includes;

a silicide layer formed on main source and drain regions and source and drain extension regions included in the source and the drain,

wherein the silicide layer which is formed on the main source and drain regions and the source and drain extension regions has a thickness in a range between 100 Å and 400 Å.

12. (Previously Presented) The straddled gate device according to claim 11, including a second silicide layer formed on electrodes of the second gate.

13. (Previously Presented) The straddled gate device according to claim 12, wherein the second silicide layer formed on the electrodes of the second gate has a thickness in a range between 100 Å and 400 Å.

14. (Previously Presented) The straddled gate device according to claim 13, wherein the silicide layer formed on the main source and drain regions and the source and drain extension regions and the second silicide layer formed on the electrodes of the second gate are of silicide of different species.

15-20. (Cancelled)

21. (Previously Presented) The straddled gate device according to claim 1, wherein when the device is in an off state (I_{off}), a length of an active channel is defined by the first gate and the second gate and when the device is in the on state (I_{on}), the length of the active channel is defined by the first gate.

22. (Previously Presented) The straddled gate device according to claim 4, includes a silicide layer formed on the main source and drain regions.

23. (Previously Presented) The straddled gate device according to claim 1, further including:

a liner interposed between the first gate and the second gate.

24. (Currently Amended) A straddled gate device formed on a semiconductor-on-insulator (SOI) substrate having active regions defined by isolation regions and an insulator layer, the device comprising:

a first gate defining a first channel region interposed between a source and a drain formed within the active region of the SOI substrate;

a second gate straddling the first gate defining second channel regions interposed between the first channel region and the source and the drain; ~~and~~

a contact connecting the first gate with the second gate~~;~~;

a first dielectric layer separating the first gate from the SOI substrate, the first dielectric layer having a relative permittivity greater than SiO_2;

a second dielectric layer separating the second gate from the SOI substrate, the second dielectric layer having a relative permittivity less than the first dielectric layer, and

a liner interposed between the first gate and the second gate,

wherein the ~~a~~ liner includes a segment separating the second gate and the SOI substrate.

25. (Previously Presented) The straddled gate device according to claim 24, wherein a dielectric layer is disposed between the segment separating the second gate and the SOI substrate.

26. (Cancelled)

27. (Previously Presented) The straddled gate device according to claim 1, wherein the SOI substrate is a fully depleted SOI (FDSOI) substrate.